CLAIMS

WHAT IS CLAIMED:

1. A method, comprising:

forming an anti-reflective coating and a resist layer on a material layer formed on a first substrate and to be patterned to define a feature in said material layer having a desired critical dimension;

determining at least one optical characteristic of said anti-reflective coating;

forming a resist feature above said anti-reflective coating by photolithography; and

reducing a size of said resist feature by performing an etch process that is controlled on the basis of an initial size of said resist feature, said desired critical dimension of said feature in said material layer and said at least one optical characteristic of said anti-reflective coating.

2. The method of claim 1, wherein said at least one optical characteristic represents at least one of a reflectivity and an extinction coefficient of said anti-reflective coating.

3. The method of claim 1, wherein controlling said etch process includes determining an etch time to reduce said size of said resist feature.

4. The method of claim 3, wherein said etch time is determined on the basis of a linear etch model.

5. The method of claim 1, further comprising etching said material layer with said resist feature having the reduced size to form said feature in said material layer.

6. The method of claim 5, further comprising determining an actual critical dimension of said feature and controlling said etch process on the basis of said actual critical dimension.

7. The method of claim 6, further comprising establishing a relationship between said at least one optical characteristic and said initial size of said resist feature to obtain at least one correction coefficient.

8. The method of claim 1, wherein said desired critical dimension is less than 100 nm.

9. The method of claim 7, wherein said etch process is controlled on the basis of a model described by the equation:

$$D_{target} = D_{initial} - a \bullet t - c\text{-}\ K \bullet R_{anti}$$

wherein D_{target} represents the desired critical dimension, $D_{initial}$ represents said initial size, K represents the correction coefficient and R_{anti} represents a measurement value of said at least one optical characteristic.

10. The method of claim 1, wherein said at least one optical characteristic of said anti-reflective coating is determined before said resist layer is formed above said anti-reflective coating.

11. The method of claim 1, wherein said at least one optical characteristic of said anti-reflective coating is determined after said resist layer is formed above said anti-reflective coating.

12. The method of claim 1, further comprising determining at least one parameter for controlling said etch process and reducing a size of a resist mask feature formed on at least one second substrate on the basis of said at least one parameter.

13. The method of claim 12, wherein said at least one parameter represents an etch time of said etch process.

14. A method of forming a gate electrode of a field effect transistor, the method comprising:

forming a gate layer stack above a substrate;

forming an anti-reflective coating on said gate layer stack;

forming a resist mask feature above said anti-reflective coating, said resist mask feature having an initial lateral size;

determining at least one optical characteristic of said anti-reflective coating;

reducing a size of said resist mask feature by performing an etch process, wherein an etch time of said etch process is controlled on the basis of said initial size, a desired critical dimension of said gate electrode and said at least one optical characteristic; and

etching said gate layer stack and said anti-reflective coating by using said resist mask feature having the reduced size as an etch mask.

15. The method of claim 14, wherein said at least one optical characteristic represents at least one of a reflectivity and an extinction coefficient of said anti-reflective coating.

16. The method of claim 14, wherein said etch time is determined on the basis of a linear etch model.

17. The method of claim 14, further comprising determining an actual critical dimension of said gate electrode and controlling said etch process on the basis of the actual critical dimension.

18. The method of claim 14, further comprising establishing a relationship between said at least one optical characteristic and said initial size of said resist feature to obtain at least one correction coefficient.

19. The method of claim 14, wherein said desired critical dimension is less than 100 nm.

20. The method of claim 14, wherein said etch process is controlled on the basis of a model described by the equation:

$$D_{target} = D_{initial} - a \bullet t - c - K \bullet R_{anti}$$

wherein D_{target} represents the desired critical dimension, $D_{initial}$ represents said initial size, K represents the correction coefficient and R_{anti} represents a measurement value of said at least one optical characteristic.

21. The method of claim 14, wherein said at least one optical characteristic of said anti-reflective coating is determined before said resist mask feature is formed above said anti-reflective coating.

22. The method of claim 14, wherein said at least one optical characteristic of said anti-reflective coating is determined after said resist mask feature is formed above said anti-reflective coating.

23. The method of claim 14, comprising determining said etch time for said substrate and using said determined etch time for forming a gate electrode on at least one further substrate.

24. An etch control system, comprising:

an etch tool; and

a control unit operatively connected to said etch tool so as to enable adjustment of a duration of at least one etch phase, said control unit being configured to receive measurement data representing a critical dimension of a resist feature and at least one optical characteristic of an anti-reflective coating, the control unit being further configured to determine an etch time for said at least one etch phase for reducing a size of said resist feature on the basis of said measurement data.